

MJPEG Decoder (v01.00.13) on HDVICP2 and Media Controller Based Platform

FEATURES

- Supports baseline sequential mode
- Supports extended sequential mode with some constraints
- Supports YUV 444, YUV 422, YUV 420, and Gray scale chroma sub-sampling formats as input (single scan as well as multiple scans)
- Supports all resolutions ranging from 32x32 to 4096x4096
- Maximum of four Huffman tables each for AC and DC DCT coefficients supported
- Supports sub-frame data synchronization for input and output buffers
- Supports slice level decoding
- Supports spatial error concealment
- Supports 8-bit and 16-bit quantization tables
- Supports YUV 444 planar, YUV 422 IBE (YUYV) and YUV 420 semi-planar chroma sub-sampling formats for output
- Supports decoding of custom Huffman tables
- Supports parsing of JFIF, Exif and comment markers
- Supports restart management for bitstream with Define Restart Interval Marker (DRI) and Restart Marker (RST)
- Supports thumbnail decoding. Thumbnail can be in JFIF or Exif marker segment. Thumbnail can be RGB as well as JPG.
- Supports scaling for YUV444 and YUV400 images
- Supports graceful exit under error conditions
- Supports Limited Pixel Range
- Does not support Arithmetic decoding
- Does not support source images of 12 bits per sample
- The other explicit features that TI's MJPEG Decoder supports are
 - eXpressDSP Digital Media (XDM IVIDDEC3) interface compliant
 - Supports multi-channel functionality
 - Supports booting of HDVICP2
 - Implements different power optimization schemes
 - Independent of any operating system
 - Ability to get plugged in any multimedia frameworks (eg. Codec Engine, OpenMax, GStreamer, etc)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Description

JPEG is an international standard for color image compression. This standard is defined in the ISO10918-1 JPEG Draft International Standard | CCITT Recommendation T .81. JPEG supports baseline sequential mode with both interleaved and non-interleaved input format and progressive mode. MJPEG (Motion JPEG) is JPEG used in video mode (for continuous image encoding/ decoding in JPEG format).

Performance and Memory Summary

This section describes the performance and memory usage of MJPEG Decoder.

Table 1 Configuration Table

CONFIGURATION	ID
Baseline Sequential interleaved decoder (4:2:0 input and 4:2:0 Semi Planar Output), sliceSwitchON = DISABLE	MJPEG_DEC_001
Baseline Sequential interleaved decoder (4:4:4 input and 4:4:4 Planar output), sliceSwitchON = DISABLE	MJPEG_DEC_002
Baseline Sequential interleaved decoder (4:2:0 input and 4:2:0 Semi Planar Output), sliceSwitchON = ENABLE	MJPEG_DEC_003
Baseline Sequential interleaved decoder (4:2:2 input and 4:2:0 Semi Planar Output), sliceSwitchON = ENABLE	MJPEG_DEC_004

Table 2 Cycles Information - Profiled on DM816x REV-A2 EVM with Code Generation Tools Version 4.5.1 for HDVICP2 and Version 5.0.3 for Media Controller .

CONFIGURATION ID	HDVICP2 PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND) ⁽¹⁾⁽⁵⁾		
	TEST DESCRIPTION ⁽²⁾	AVERAGE ⁽³⁾	PEAK ⁽⁴⁾
MJPEG_DEC_001	davincieffect_qcif_yuv420_sp.jpeg (176 x 144, Baseline Sequential)	6.13	6.46
	flower_cif_420.jpeg (352x288, Baseline Sequential)	10.16	10.4
	jump_640x352_420sp.jpeg (640x352, Baseline Sequential)	16.33	16.55
	fire_D1_420sp.jpeg (720x480, Baseline Sequential)	22.6	22.83
	pedestrian_1920x1080p_420sp.jpeg (1920 x 1080, Baseline Sequential)	112.60	113.10
MJPEG_DEC_002	bus_352x288_444.jpeg (352x288, Baseline Sequential)	16.27	16.51
	container_720x576_444.jpeg (720 x 576, Baseline Sequential)	51.39	51.59
	pedestrian_1920x1080_444.jpeg (1920 x 1088, Baseline Sequential)	235.49	235.70
MJPEG_DEC_003	pedestrian_720p_420.jpeg (1280x720, Baseline Sequential) with numSwitchPerFrame = 1	52.41	52.50
	pedestrian_720p_420.jpeg (1280x720, Baseline Sequential) with numSwitchPerFrame = 2	55.83	56.12
	pedestrian_720p_420.jpeg (1280x720, Baseline Sequential) with numSwitchPerFrame = 3	58.8	59.10
	pedestrian_720p_420.jpeg (1280x720, Baseline Sequential) with numSwitchPerFrame = 4	61.70	62.03
	pedestrian_1080p_420.jpeg (1920x1080, Baseline Sequential) with numSwitchPerFrame = 1	112.60	113.10
	pedestrian_1080p_420.jpeg (1920x1080, Baseline Sequential) with numSwitchPerFrame = 2	115.87	116.02
	pedestrian_1080p_420.jpeg (1920x1080, Baseline Sequential) with numSwitchPerFrame = 3	118.78	118.96
	pedestrian_1080p_420.jpeg (1920x1080, Baseline Sequential) with numSwitchPerFrame = 4	120.94	121.86
MJPEG_DEC_004	lambhorgini_1280x720_422yuyv.jpg (1280x720, Baseline Sequential) with numSwitchPerFrame = 1	70.83	71.40
	lambhorgini_1280x720_422yuyv.jpg (1280x720, Baseline Sequential) with numSwitchPerFrame = 2	74.27	74.82
	lambhorgini_1280x720_422yuyv.jpg (1280x720, Baseline Sequential) with numSwitchPerFrame = 3	77.29	77.74
	lambhorgini_1280x720_422yuyv.jpg (1280x720, Baseline Sequential) with numSwitchPerFrame = 4	80.19	80.66
	pedestrian_1080p_422ibe.jpg (1920x1080, Baseline Sequential) with numSwitchPerFrame = 1	152.93	153.12
	pedestrian_1080p_422ibe.jpg (1920x1080, Baseline Sequential) with numSwitchPerFrame = 2	156.41	156.57
	pedestrian_1080p_422ibe.jpg (1920x1080, Baseline Sequential) with numSwitchPerFrame = 3	159.35	159.52
	pedestrian_1080p_422ibe.jpg (1920x1080, Baseline Sequential) with numSwitchPerFrame = 4	162.27	162.46

(1) Measured on DM816x REV-A2 EVM having Cortex-A8 @ 1GHz, HDVICP2 @ 533MHz, Media Controller @ 250 MHz, L3 interconnect @ 500 MHz and DDR2 @ 400 MHz and there could be a variation of around 1-2% in the numbers.

- a) Media Controller code is placed in cacheable memory region in DDR.
- b) No latency from system at process call and processing unit as frame (no sub-frame level communication) is assumed.
- c) All Luma 2D Video buffers of codec being in TILED_8 Bit Memory and all Chroma 2D Video buffers of codec being in TILED_16 Bit Memory

(2) Streams have been compressed with Quantization Tables and Huffman Tables suggested in the JPEG Standard document.

(3) Average is computed based on worst case cycles having 2 extra output frame buffer. Average is calculated @ 30fps

- (4) Peak is based on worst case cycles having no extra output frame buffer. It is computed based on peak among 30 frames @30fps.
- (5) Cycles measured for positive streams. Decoding error streams of same resolution with error concealment enabled will consume significantly higher Mega cycles.

Table 3 Memory Statistics of Media Controller - Generated with Code Generation Tools Version 5.0.3

CONFIGURATION ID	RESOLUTION	PROGRAM MEMORY	MEMORY STATISTICS ⁽¹⁾						TOTAL
			INTERNAL	DATA MEMORY				STACK	
				EXTERNAL ⁽²⁾			CONST		
				PERSISTENT ⁽³⁾					
				TILED8 (numBufs x Width x Height)	TILED16 (numBufs x Width x Height)	TILED PAGE / RAW			
MJPEG_DEC_001 MJPEG_DEC_002 MJPEG_DEC_003 MJPEG_DEC_004	All	13	0	0	0	13	255	2	283

- (1) All memory requirements are expressed in kilobytes (1 K-byte = 1024 bytes) and there might be rounding to next integer K-byte. Stack can be kept in internal/external memory, negligible performance impact can be observed in Media Controller cycles if it is placed in external memory.
- (2) Codec's request of memory container can be over-riden by application, adhering to the below rules
 - a. TILED PAGE can be overridden by RAW
 - b. TILED8, TILED16 can be overridden by TILED PAGE, RAW
 - c. TILED16 can be overridden by TILED8, RAW, TILED PAGE
 However, in case of overriding of 2B and 2C, there can be some performance impact.
- (3) Persistent memory is instance specific and does not include I/O buffers.

Table 4 Split-up of Media Controller Internal Data Memory Statistics

CONFIGURATION ID	DATA MEMORY - INTERNAL ⁽¹⁾		
	SHARED		INSTANCE
	CONSTANTS	SCRATCH	
MJPEG_DEC_001, MJPEG_DEC_002, MJPEG_DEC_003, MJPEG_DEC_004	0	0	0

- (1) Internal memory refers to on chip memory. If the system doesn't have enough internal memory, then external memory can also be used. Memory requirements are expressed in kilobytes.

Notes

- I/O buffers:
 - Input buffer size = 3060 KB (assuming worst case for 1920x1088, YUV444 image)
 - Output buffer size = 6120 KB (for 1920x1088, YUV444 image)
- None of the buffers at input and output level is accessed by Media Controller processor hence the data should be valid in DDR (not in cache)
- Total data memory for N non pre-emptive instances = Constants + Runtime Tables + Scratch + N * (Instance + I/O buffers + Stack)
- Total data memory for N pre-emptive instances = Constants + Runtime Tables + N * (Instance + I/O buffers + Stack + Scratch)
- MAIL BOX FIFO #0 and #1 are used and user numbering for Media Controller as 2 and for HDVICP2 as 3 is assumed
- It is assumed that RTS library from ARM is available in system because few symbols like

- memcpy are used in codec
- All constants and Input/Output Buffers to decoder are assumed to be in VDMA addressable space in DDR

References

- ITU-CCITT recommendation T.81 (reproduction of ISO/IEC 10918-1)
- eXpressDSP Algorithm Interoperability Standard (TMS320 Algorithm Interface Standard)
- MJPEG Decoder on HDVICP2 and Media Controller Based Platform User's Guide

Glossary

Term	Description
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

Acronyms

Acronym	Description
CCITT	Committee Consultative International Telephone and Telegraph
DCT	Discrete Cosine Transform
DRI	Define Restart Interval Marker
DSP	Digital Signal Processing
IEC	International Electrotechnical Commission
ISO	International Organization for Standardization
ITU	International Telecommunication Union
JFIF	JPEG File Interchange Format
JPEG	Joint Photographic Experts Group
MJPEG	Motion JPEG
RST	Restart Marker
XDM	eXpressDSP Digital Media

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have not been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive & Transportation	www.ti.com/automotive
Communications & Telecom	www.ti.com/communications
Computers & Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energyapps
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics & Defense	www.ti.com/space-avionics-defense
Video & Imaging	www.ti.com/video

TI E2E Community e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright© 2014, Texas Instruments Incorporated