AIF2 Low-level Driver

Dual mode test case

Applies to Product Release: 01.00.00.15:
Publication Date: May, 2013

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Table of Contents

Introduction

AIF2 lack of flexibility:

AIF2 is designed to support WCDMA antenna traffic by using DIO engine, which can interface directly with RAC and TAC.

AIF2 support LTE antenna traffic by using PKTDMA, which can connect directly to FFTC.

The problem is that within AIF2, PKTDMA and DIO engine cannot co-exist. This lead to only two possibilities to support simultaneous traffic using AIF2: use DIO engine to support both LTE and WCDMA, or use the PKTDMA. AIF2LLD is focused on the DIO engine solution.

AIF2 configuration

For dual mode, the AIF2LLD dedicate link for WCDMA or LTE. Both traffics can't be set for the same links. For WCDMA traffic, as we are using DIO engine, the AIF2 configuration is identical. The effort is for LTE part, where we have to configure the DIO and timing to fit LTE requirements.

PE & PD: For Protocol decoder and protocol encoder point of view, the way to configure the AxCs is independent of the data transport mechanism used (DIO or PKTDMA). So the logic behind this configuration hasn't change from WCDMA and LTE test examples. The only difference here that can be mentioned is the configuration of two PdFrameTc and PeframeTc per link. The first one is used for LTE AxCs and is configure likewise (140 symbols in a frame) and the second for WCDMA (15 slots in one frame).

DB: data buffer are bigger for dual mode than for WCDMA mode. Global DIO buffer length is 128 bytes for WCDMA against 256 bytes for dual mode.

Configuration for both ingress and egress:

	data swap	IQ order
LTE	DB word swap	no IQ swap
WCDMA UL	DB byte swap	no IQ swap
WCDMA DL	DB word swap	no IQ swap

AT timer setup: As we are using DIO mode, all the timings are WCDMA based. The RadClockCountTC is set to match one WCDMA slot (frame TC divide by 15).

Dio engine:

For LTE 20MHz, DIO engine needs to service 4 QW every 2 chips (520ns), whereas for WCDMA, it needs to trig every 4 chips or 8 chips. For LTE, the DIO event modulo should be set to match 2 chips.

DIO event modulo:

	WCDMA UL	WCDMA DL	LTE
Modulo	8 chips	4 chips	2 chips

For dual mode, the LLD setup 3 AT events:

- Event 7: frame based event. (10 ms)
- Event 5: timeslot based event. This is used for LTE re-packetization (see below for more detail).
- Event 6: LTE symbol based event. This timer is used to trigger the EDMA3 that is in charge of pushing packet (see EDMA section for details).

Memory challenge

Memory requirement for LTE with DIO

LTE normal cyclic prefix mode has long and short cyclic prefix length, so the symbol length is not a constant. Unfortunately, DIO uses a circular buffer to read and write data. One solution would be to use slot based buffer as the DIO buffer, however it is too memory consuming: LTE 20MHz would need 61440 bytes per antenna.

Instead, the AIF2 LLD prefers that the DIO buffer aligns with the LTE antenna traffic periodically so that it is easier for the application to manage the antenna symbol location. The period is preferred to be slot, subframe or a few subframes. For Lte 20MHz, examples of buffer sizes of 5120 samples or 6144 samples satisfy the above requirement:

- DIO buffer 6144 aligns with the subframe periodically
- DIO buffer 5120 aligns with the slot periodically

AIF2 LLD chooses the DIO buffer of 5120 samples, so the application is slot based (AT Event 5).

LTE antenna data placement in DIO buffer

For normal cyclic prefix case, as the DIO buffer doesn't always align with the antenna symbol, instead it only aligns with the slot, some antenna symbols would contain two segments of the data in the DIO buffer.

LTE 20MHz antenna symbol placement in DIO buffer for normal cyclic prefix case.

	Num of Segments	Seg 1 offset (samples)	Seg 1 len (samples)	Seg 2 offset (samples)	Seg 2 len (samples)
sym 0	1	0	2208		
sym 1	1	2208	2192		
sym 2	2	4400	720	0	1472
sym 3	1	1472	2192		
sym 4	2	3664	1456	0	736
sym 5	1	736	2192		
sym 6	1	2928	2192		
sym 7	1	0	2208		
sym 8	1	2208	2192		
sym 9	2	4400	720	0	1472
sym 10	1	1472	2192		
sym 11	2	3664	1456	0	736
sym 12	1	736	2192		
sym 13	1	2928	2192		

In order to map this scheme, the LLD use host descriptor that are linked for the symbols with 2 segments.

Application usage

A Zero CPU intervention is desired to connect AIF2 and FFTC in the case of using DIO:

On Ingress:

- Since antenna data placement is regular, packet descriptors can be pre-configured to point to the corresponding position for each symbol
- For the symbols with two segments, the packet descriptors can be pre-linked
- The pre-configured the descriptors can be arranged in a queue in the order of the antenna symbols
- EDMA can be used to pop the pre-arranged descriptor from the queue and push it to the input queue of FFTC to achieve zero CPU intervention (see EDMA section for details)
    - To maintain synchronization, EDMA should be triggered based on AT event
    - As AT events are not tied with data transfer and availability, it is the responsibility of the application to set the AT event with enough margin to guarantee the data availability (vs. in pktDMA case descriptor pushed into the Rx Q guarantees data availability)

On egress (not implemented in AIF2 LLD dual mode test case):

- Rx FDQ of FFTC should be arranged to have the descriptors pointing to the buffers that matches the DIO data placement

- The FFTC Rx Q can be set to use one of the infra-structure DMA Tx Q, so that the descriptors can be disjointed and recycled to the Rx FDQ correctly without CPU intervention
    - Need to check if the reclamation queue have the functionality of disjointing descriptors

AIF2 DIO facts

- The real time aspect of the antenna traffic requires DIO engine
    - to read and write 4 QW per antenna carrier every 520ns for LTE 20MHz
    - to read 1 QW per antenna carrier every 4 chips (1041ns) and to write 2 QW per antenna carrier every 8 chips of time (2083ns) for WCDMA
- DIO engine can be programmed to have burst of 1 QW, 2 QW or 4 QW burst. Each burst of 4 QW requires 6 VBUS cycles to complete if there is no stalling
    - All AxCs on the same DIO engine need to be configured the same
    - For WCDMA, doing burst of 4 QW requires antenna carriers to be contiguous
    - If some antennas are not used for whatever reasons, burst of 4 QW can still be used to read/write which includes dummy data of the non-used antenna carriers
- There are 3 DIO engines in AIF2 with DIO engine 0 having the highest priority
    - Prefer to use DIO engine 0 for LTE antenna traffic and use the other DIO engines for WCDMA antenna traffic
- All the AxCs serviced on the same DIO engine will be triggered at the same time
    - The more antenna carriers the worse the peak throughput, although the average throughput could be same

FFTC interface challenge: EDMA configuration

In order to achieve zero CPU intervention on ingress, it is required to configure the EDMA3 to pop and push the pre-configured descriptor that point to the DIO buffer that contains the LTE data. The EDMA should be triggered every symbol and need an AT event dedicated for this task.

The AT event 6 is configured at a symbol pace, and will be used to trigger the first EDMA3 channel that is mapped for LTE AxC0. LTE AxC1's EDMA3 channel will be chained in completion of that transfer so do all the next LTE channels.

EDMA3 specific configuration:

TCI6614:

- EDMA CC1
- TC 3
- EDMA3 channel synchronization event: 16 (AIF radio timing sync event 6) trig AxC0.
- EDMA3 channel synchronization event: 17 (trig in completion of channel 16) trig AxC1.

TCI6638K2K & K2H:

- EDMA CC2
- TC 0
- EDMA3 channel synchronization event: 22 (AIF radio timing sync event 6) trig AxC0.
- EDMA3 channel synchronization event: 23 (trig in completion of channel 16) trig AxC1.