AIF2 LLD

Driver architecture for multiple software stacks

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SW stack needs for Cpri traffic

- Different SW stacks need to access AIF2 resources simultaneously
  - Lte, Wcdma, Ethernet fast C&M
- AIF2 needs to be programmed at once during application initialization.
- AIF2 has 2 DMA modes:
  - DIO xor PKTDMA
  - When applications co-exist on the same device, only one mode selected
  - DIO recommended for Dual Lte/Wcdma Mode
- Different stacks can generate traffic for the same AIF2 link, or different ones.
  - Antenna IQ and Cpri control words can be on the same link
- Applications have also different timing needs
  - That influences the programming of AIF2 radio timers
  - AT events are also shared resources.
- That implies that the different applications need a mechanism to describe their AIF2 resource needs, and in return, get access to a specific resource, for instance a Dio engine number, or a Pktdma/HW queue

Current SW stack limitations

- The current implementation of L1 stacks SW is interleaved with AIF2 configuration for CPRI link
  - CPRI link setup procedure has been implemented as part of L1 SW
  - It is performed after receiving FAPI PHY START message from L2
- Such a startup sequence is creating following issues in the overall system
  - CPRI link setup is dependent on L1 SW (not practical for a RRH)
  - CPRI link is down whenever L1 SW suspends/crashes (should not be the case)
  - Any reconfiguration/reset of L1 SW requires complete CPRI link setup/synchronization to be repeated and thus creating delays in reconfiguration/reset
- LTE RRH case: from the overall eNB layers startup procedure the FAPI PHY START message is tied to Cell Setup trigger, so unless the Cell setup command is complete- L1 SW cannot come up which in turn shall enable the CPRI link and thus the Communication with Radio head cannot be started unless the Cell setup is complete. This essentially means that radio head software download, radio head configuration cannot be performed till cell setup is complete. Communication link with radio head is lost whenever L1 SW is down as the CPRI link is also down.

Multi-stack scenarios of interest

- Small cell Lte and Wcdma simultaneous traffic
  - 1 AIF2 4x link for Lte, 1 AIF2 4x link for Wcdma
  - AIF2 DIO mode for both traffic
  - AIF2 interfaces to FFTC, RAC,TAC, and DDR/SL2
- Small cell Lte and Ethernet Fast C&M
  - Same AIF2 4x link for both types of traffic
  - AIF2 PKTDMA mode for both traffic
  - AIF2 interfaces to FFTC and DDR/SL2

Implementation proposal

- De-couple AIF2 configuration from Lte and Wcdma L1 software
- One instance of AIF2 LLD across all applications
  - Place AIF_ConfigObj in shared memory section and let AIF2 LLD manage it
- AIF2 register handling
  - Centralized configuration and AIF2 exception monitoring
    - Only one DSP core will perform the actual programming of AIF2 registers
    - Only one DSP core manages AIF2 exceptions, and then need a notification/alarm mechanism to the different stacks
- Application interfaces
  - Init time
    - AIF_ResDescObj describes in one structure the needs from all stacks (mode, link number, number of AxCs, dio engine number, …)
    - Each stack gets the configuration during init time and is in charge of configuring its DMA parameters (PktDMA or DIO)
  - Runtime
    - Stacks get radio timer info thru specific lld APIs
    - To push/pop/recycle packets, this is done thru qmss lld using fields from the AIF_ConfigObj
- Sync points across all cores:
  - For init/get resources from AIF_ResDescObj
  - Prior to AIF_initHw()

Architecture Diagram